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DATA SHEET

TEA0675
Dual Dolby* B-type noise reduction circuit for playback applications

Preliminary specification
Supersedes data of July 1993
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Philips Semiconductors

PHILIPS

Dual Dolby* B-type noise reduction circuit for playback applications

TEA0675

FEATURES

- Dual noise reduction (NR) channels
- Head pre-amplifiers
- Reverse head switching
- Automatic Music Search (AMS)
- Music scan
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV
- 24 pins
- Improved EMC behaviour.

GENERAL DESCRIPTION

The TEA0675 is a bipolar integrated circuit that provides two channels of Dolby B noise reduction for playback applications in car radios. It includes head and equalization amplifiers with electronically switchable time constants. Furthermore it includes electronically switchable inputs for tape drivers with reverse heads.

This device also detects pauses of music in the Automatic Music Search (AMS) scan mode, for applications with an intelligent controlled tape driver, or AMS-latch mode, for applications with a simple controlled tape driver. For both modes, the delay time can be fixed externally by a resistor. The device operates with power supplies in the range of 7.6 to 12 V, output overload level increasing with increase in supply voltage.
Current drain varies with the following variables:

supply voltage

noise reduction on/off

AMS on/off.

Because of this current drain variation it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	–	12	V
I_{CC}	supply current	–	26	31	mA
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA0675	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
TEA0675T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

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BLOCK DIAGRAM

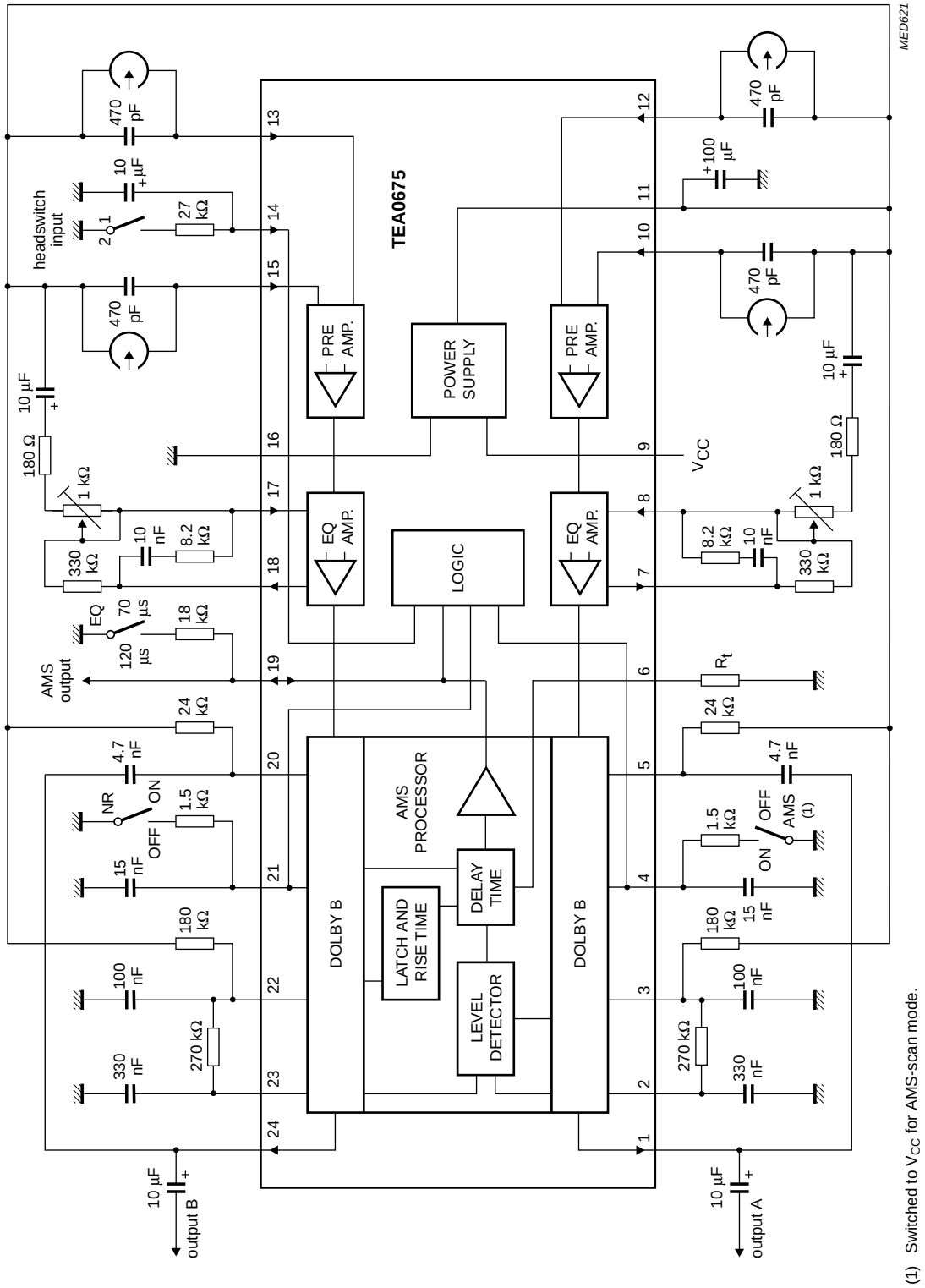


Fig.1 Block and application diagram.

(1) Switched to V_{CC} for AMS-scan mode.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
INTA	2	integrating filter channel A
CONTRA	3	control voltage channel A
HPA	4	high-pass filter channel A
SCA	5	side chain channel A
TD	6	delay time constant
EQA	7	equalizing output channel A
EQFA	8	equalizing input channel A
V_{CC}	9	supply voltage
INA1	10	input channel A1 (forward or reverse)
V_{ref}	11	reference voltage
INA2	12	input channel A2 (reverse or forward)
INB2	13	input channel B2 (reverse or forward)
HS	14	head switch input
INB1	15	input channel B1 (forward or reverse)
GND	16	ground
EQFB	17	equalizing input channel B
EQB	18	equalizing output channel B
AMSEQ	19	AMS output and EQ switch input
SCB	20	side chain channel B
HPB	21	high-pass filter channel B
CONTRB	22	control voltage channel B
INTB	23	integrating filter channel B
OUTB	24	output channel B

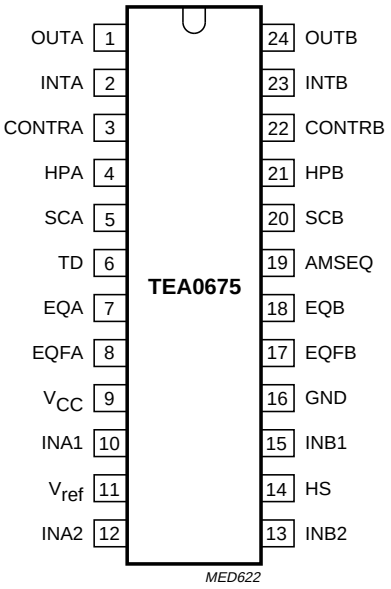


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Noise Reduction (NR) is enabled when pin HPB is open-circuit and disabled when connected to GND via an 1.5 kΩ resistor.

Dolby B noise reduction only operates correctly if 0 dB Dolby level is adjusted at 387.5 mV.

Automatic Music Search (AMS) scan mode is enabled when pin HPA is connected to V_{CC} via an 1.5 kΩ resistor and disabled when pin HPA is open-circuit. Switching AMS on, internally NR is switched OFF simultaneously (see Figs 5 and 6 for principle timing in AMS-scan mode).

AMS-latch mode is enabled when pin HPA is connected to GND via an 1.5 kΩ resistor and disabled when pin HPA is open-circuit. Switching AMS on, NR is switched off internally. In this mode the device detects a pause level signal, when a music level signal has appeared first (see Figs 7 and 8 for principle timing). Furthermore a longer rise time constant is supplied for suppressing the detection of plops on tape. The output signal at pin AMSEQ in this mode may be applied to drive a tape driver logic circuit.

Equalization time constant switching (70 μs or 120 μs) is achieved when pin AMSEQ is connected to GND via an 18 kΩ resistor (120 μs), or left open-circuit (70 μs). This does not affect the AMS output signal during AMS mode (see Fig.1).

Head switching is achieved when pin HS is connected (input IN2 active) to GND via a 27 kΩ resistor, or left open-circuit (input IN1 active). The 10 μF capacitor at pin HS sets the time constants for smooth switching.

In AMS mode the signals of both channels are rectified and then added. This means, even if one channel signal appears inverted to the other channel, the normal AMS function is ensured. Pins HPB and HPA perform the function of a logic input for AMS, respectively NR mode switching in both channels and provide the frequency dependent feedback of the control chain amplifier in the corresponding channel. Thus it is important that no voltage is applied to pins HPB and HPA during NR on/AMS off mode, otherwise this will cause irregular NR characteristics.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	14	V
V_i	input voltage (except pin 11)		–0.3	$+V_{CC}$	V
t_{short}	pin 11 (V_{ref}) to V_{CC} short-circuiting duration		–	5	s
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage for all pins	note 1	–2	+2	kV
		note 2	–500	+500	V

Notes

1. Human body model (1.5 kΩ, 100 pF).
2. Machine model (0 Ω, 200 pF).

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = 25 °C; all levels are referenced to 387.5 mV (RMS) (0 dB) at test point (TP) pin OUTA or OUTB; see Fig.1; NR on/AMS off; EQ switch in the 70 μs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.6	10	12	V
I_{CC}	supply current		–	26	31	mA
α_m	channel matching	f = 1 kHz; V_o = 0 dB; NR off	–0.5	–	+0.5	dB
THD	total harmonic distortion (2nd and 3rd harmonic)	f = 1 kHz; V_o = 0 dB	–	0.08	0.15	%
		f = 10 kHz; V_o = 10 dB	–	0.15	0.3	%
H_R	headroom at output	V_{CC} = 7.6 V; THD = 1%; f = 1 kHz	12	–	–	dB
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	internal gain 40 dB, linear; CCIR/ARM weighted; decode mode; see Fig.25	78	84	–	dB
PSRR	power supply ripple rejection	$V_{i(rms)}$ = 0.25 V; f = 1 kHz; see Fig.22	52	57	–	dB
f_o	frequency response; referenced to TP	encode mode; see Fig.25				
		V_o = –25 dB; f = 0.2 kHz	–22.9	–24.4	–25.9	dB
		V_o = 0 dB; f = 1 kHz	–1.5	0	+1.5	dB
		V_o = –25 dB; f = 1 kHz	–17.8	–19.3	–20.8	dB
		V_o = –25 dB; f = 5 kHz	–18.1	–19.6	–21.1	dB
		V_o = –35 dB; f = 10 kHz	–24.4	–25.9	–27.4	dB
α_{cs}	channel separation	V_o = 10 dB; f = 1 kHz; see Fig.23	57	63	–	dB
α_{cc}	crosstalk between active and inactive input	f = 1 kHz; V_o = 10 dB; NR off; see Fig.23	70	77	–	dB
R_L	load resistance at output	AC-coupled; f = 1 kHz; V_o = 12 dB; THD = 1%	10	–	–	kΩ
G_v	voltage gain of pre-amplifier	from pin INA1 or INA2 to pin EQFA and from pin INB1 or INB2 to pin EQFB; f = 1 kHz	29	30	31	dB
$V_{I(offset)(DC)}$	DC input offset voltage		–	2	–	mV
$I_{i(bias)}$	input bias current		–	0.1	0.4	μA
R_{EQ}	equalization resistor		4.7	5.8	6.9	kΩ
R_i	input resistance head inputs		60	100	–	kΩ
A_v	open-loop amplification	pin INA1 or INA2 to pin EQA and pin INB1 or INB2 to pin EQB				
		f = 10 kHz	80	86	–	dB
		f = 400 Hz	104	110	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{ref} - V_{OUT}$	DC output offset voltage at pins OUTA and OUTB	NR off; pins INA1, INA2, INB1 and INB2 connected to V_{ref}	–0.15	–	+0.15	V
I_O	DC output current	pin OUTA to ground	–2	–	–	mA
		pin OUTB to V_{CC}	0.3	–	–	mA
Z_o	output impedance		–	80	100	Ω
$V_{no(rms)}$	equivalent input noise voltage (RMS value)	NR off; unweighted; f = 20 Hz to 20 kHz; R_{source} = 0 Ω	–	0.7	1.4	μV
V_{TD}	AMS timing (DC level)	resistor R_t connected to pin TD	V_{CC} – 3	–	V_{CC}	V
EMC	DC offset voltage at pins OUTA and OUTB	f = 900 MHz; $V_{i(rms)}$= 6 V; see Figs 26, 27 and 28	–	40	–	mV
Switching thresholds						
V_{NROFF}	voltage at HPB (pin 21)	NR off	$0.19V_{CC}$	$0.23V_{CC}$	$0.25V_{CC}$	V
I_{NROFF}	output current	NR off	–	–0.7	–1	mA
I_{NRON}	input current	NR on	–	open	200	nA
$V_{HPB(max)}$	maximum voltage		–	–	$0.75V_{CC}$	V
HPA (PIN 4)						
V_{AMSlON}	pin voltage	AMS-latch on	$0.19V_{CC}$	$0.23V_{CC}$	$0.25V_{CC}$	V
I_{AMSlON}	output current		–	–0.7	–1	mA
V_{AMSsON}	pin voltage	AMS-scan on	$0.75V_{CC}$	$0.77V_{CC}$	$0.81V_{CC}$	V
I_{AMSsON}	input current		–	0.8	1	mA
I_{AMSOFF}	pin current	AMS off	–	open	200	nA
$V_{HPA(max)}$	maximum voltage		–	–	$0.75V_{CC}$	V
AMSEQ (PIN 19)						
AMS output (AMS mode)						
V_{OH}	HIGH level output voltage		4	4.6	5	V
I_{OH1}	HIGH level output current	note 1	+10	–	–150	μA
I_{OH2}	HIGH level output current	note 1	+0.01	–	–1	mA
t_d	minimum pulse width; delay time range	see Table 1	–	23 to 160	–	ms
V_{OL}	LOW level output voltage		–	0.1	0.7	V
I_{OL}	LOW level output current		–0.02	–	+1	mA
t_r	minimum pulse width rise time	AMS-scan mode	2	6	10	ms
		AMS-latch mode	130	150	170	ms
$A_{M/P}$	signal level at output for AMS switching music to pause	AMS mode; f = 10 kHz; note 2; see Fig.24	–25	–22	–19	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$A_{P/M}$	signal level at output for AMS switching pause to music	AMS mode; f = 10 kHz;	–24	–21	–18	dB
EQ switch input (not AMS mode)						
I_{EQ70}	input current	time constant 70 μs active	–150	–	–	μA
I_{EQ120}	input voltage	time constant 120 μs active	–1000	–	–250	μA
I_{EQth}	threshold current	note 1	–	–200	–	μA
HEAD SWITCHING						
V_{HSW}	pin voltage	load current +90 to –90 μA	–	$0.8V_{CC}$	–	V
I_{HSW}	input current	V_{HSW} = 0 to V_{CC}	–170	–	+170	μA
$V_{HSW(HIGH)}$	HIGH level pin voltage	inputs INA1 and INB1 active; note 3	$\frac{1}{2}V_{CC}$ + 0.5	–	V_{CC}	V
$V_{HSW(LOW)}$	LOW level pin voltage	inputs INA2 and INB2 active	0	–	$\frac{1}{2}V_{CC}$ – 0.5	V

Notes

1. In AMS off mode, pin AMSEQ is HIGH level, the equalization time constant will be switched by pulling approximately 200 μA out of pin AMSEQ. This means for the device connected to pin AMSEQ, a restriction of input current at HIGH level less than 200 μA during AMS off; otherwise the selection of the equalization time constant is disabled and fixed at 120 μs. If the connected devices consume more than 200 μA, this input has to be disconnected in AMS off mode. (To ensure switching, the currents for the different switched modes are specified with a tolerance of ±50 μA in Chapter “Characteristics”.) For an application with a fixed EQ time constant of 120 μs the equalizing network may be applied completely external. Change 8.2 kΩ resistor to 14 kΩ the internal resistor R_{EQ} = 5.8 kΩ is short-circuited by fixing the EQ switch input at the 70 μs position (I_{EQ70}).
2. The high speed of the tape (FF, REW) at the tape head during AMS mode causes a transformation of level and frequency of the originally recorded signal. It means a boost of signal level of approximately 10 dB and more for recorded frequencies from 500 Hz up to 4 kHz. So the threshold level of –22 dB corresponds to signal levels in Play Back (PB) mode of approximately –32 dB. The AMS inputs for each channel are pin SCA and pin SCB. As the frequency spectrum is transformed by a factor of approximately 10 to 30 due to the higher tape speed in FF, REW, the high-pass filter (4.7 nF/24 kΩ) removes the effect of offset voltages but does not affect the music search function.

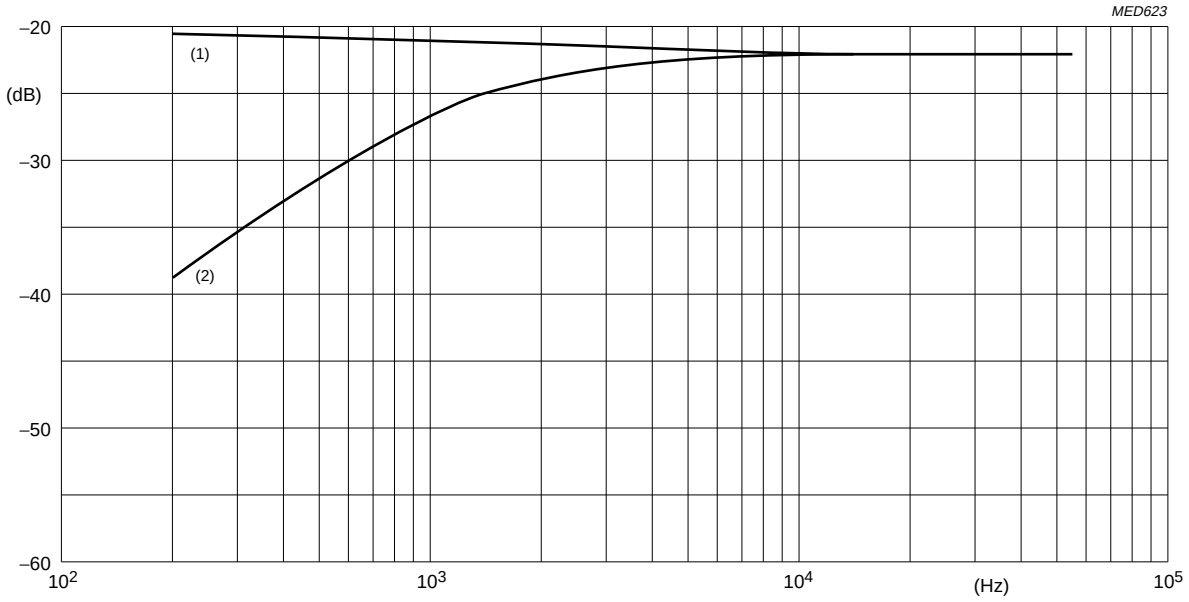
   In the application circuit (Fig.1) the frequency response of the system between tape heads input, e.g. pins INA2 and INB2, to the AMS input pins SCA and SCB is constant over the whole frequency range (see Fig.3).
3. To activate the inputs IN1, pin HS might be left open-circuit. In this event the DC level at pin HS is $0.775V_{CC}$.

Table 1 Blank delay time set by resistor R_t at pin TD

RESISTOR VALUE R_t (kΩ)	DELAY TIME t_d TYP. (ms)	TOLERANCE (%)
68	23	20
150	42	15
180	48	15
220	56	15
270	65	10
330	76	10
470	98	10
560	112	10
680	126	10
820	142	10
1000	160	10

General note

It is recommended to switch off V_{CC} with a gradient of 400 V/s at maximum to avoid plops on tape in the event of contact between tape and tape head while switching off.



(1) AMS threshold level for application circuit (Fig.1).
(2) AMS threshold level for test circuit (Fig.24).

Fig.3 AMS threshold level.

Short description ‘music search’

A system for ‘music search’ mainly consists of a level and a time detection (see Fig.4). For adapting and decoupling the input signal will be amplified (A), then rectified (B) and smoothed with a time constant (C). So the voltage at (C) corresponds to the signal level and will be compared to the predefined pause level at the first comparator (D), the level detector. If the signal level becomes smaller than the pause level, the level detector changes its output signal. Due to the output level of the level detector the capacitor of the second time constant (E) will be charged, respectively discharged. If the pause level of the input signal remains for a certain time, the voltage at the capacitor reaches a certain value, which corresponds to an equivalent time value. The voltage at the capacitor will be compared to a predefined time-equivalent voltage by the second comparator (F), the time detector. If the pause level of the input signal remains for this predefined time, the time detector changes its output level for ‘pause found’ status.

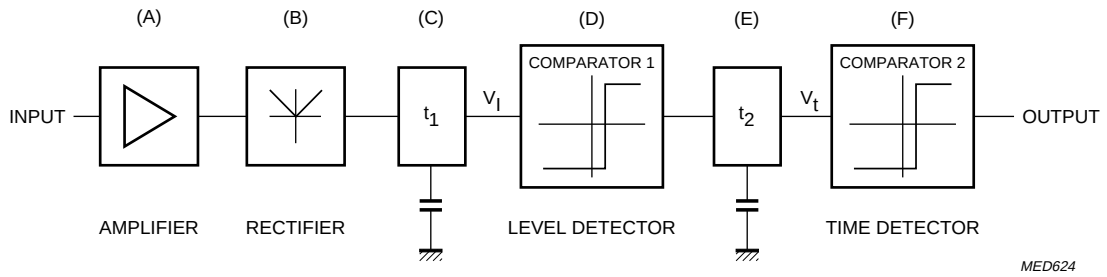


Fig.4 Integrated ‘music search’ function.

Description of the principle timing diagram for AMS-scan mode without initial input signal (see Fig.5)

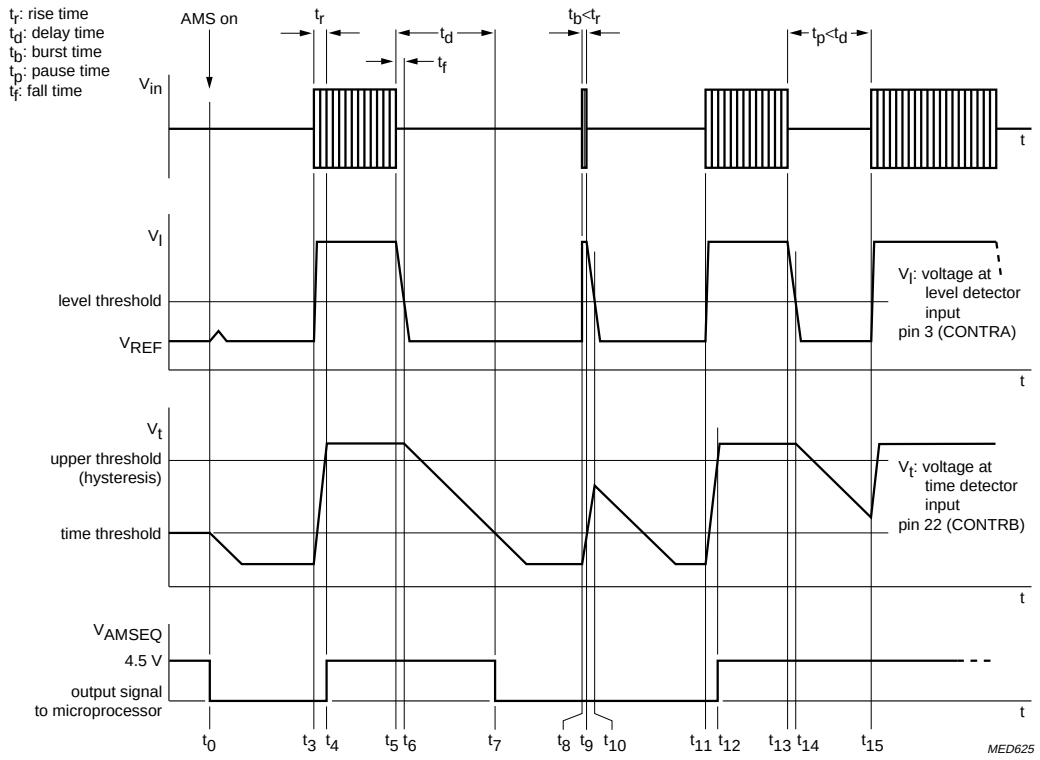


Fig.5 AMS-scan mode without initial input signal.

By activating AMS-scan mode, the AMS output level directly indicates whether the input level corresponds to a pause level (V_{AMSEQ} = LOW) or not (V_{AMSEQ} = HIGH). At t_0 the AMS-scan mode is activated. Without a signal at V_{in}, the following initial procedure runs until the AMS output changes to LOW level: due to no signal at V_{in} the voltage at the level detector input V_l (pin 3, CONTRA) remains below the level threshold and the second time constant will be discharged (time detector input V_t). When V_t passes the time threshold level, the time detector output changes to LOW level. Now the initial procedure is completed.

If a signal burst appears at t_3, the level detector input voltage rises immediately and causes its output to charge the second time constant, which supplies the input voltage V_t for the time detector. When V_t passes the upper threshold level after the rise time t_r (at t_4), the AMS output changes to HIGH. If the signal burst ends at t_5 the level detector input V_l falls to its LOW level. When passing the level threshold at t_6, the discharging of the second time constant begins. Now the circuit measures the delay time t_d, which is externally fixed by a resistor and defines the length of a pause to be detected. If no signal appears at V_{in} within the time interval t_d, the time detector output switches the AMS output to LOW level at t_7.

If a plop noise pulse appears at V_{in} (t_8) with a pulse width less than the rise time $t_r > t_b$, the plop noise will not be detected as music. The AMS output remains LOW.

Similarly the system handles ‘no music pulses’ t_p: when music appears at t_{11} with a small interruption at t_{13}, this interruption will not affect the AMS output for $t_p < t_d$.

Description of the principle timing diagram for AMS-scan mode with initial input signal (see Fig.6)

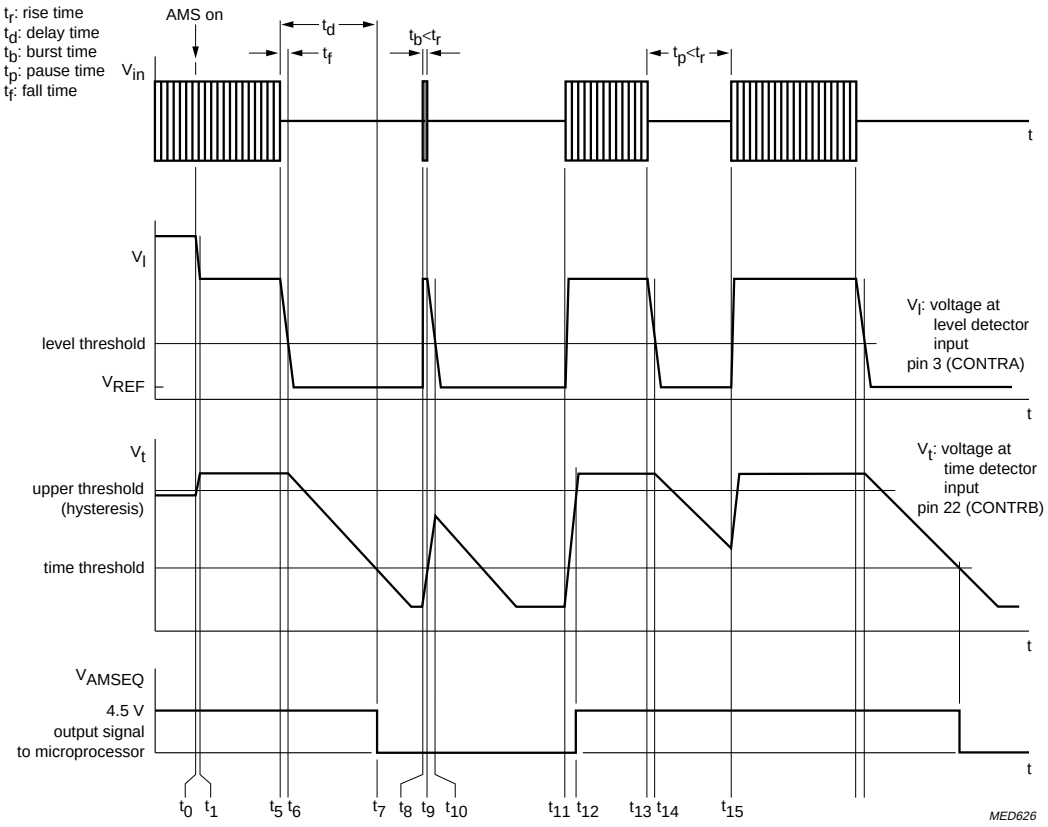


Fig.6 AMS-scan mode with initial input signal.

At t_0 the AMS-scan mode is activated. With an input signal at V_{in}, the following initial procedure runs until the circuit gets a steady state status.

Due to the signal at V_{in} the voltage at the level detector input V_l (pin 3, CONTRA) slides to a value which is defined by a limiter. This voltage causes the level detector output charging the second time constant (time detector input V_t) to its maximum voltage level at t_1. Now the initial procedure is completed.

The following behaviour does not differ from the description in Section “Description of the principle timing diagram for AMS-scan mode without initial input signal (see Fig.5)”.

Description of the principle timing diagram for AMS-latch mode without initial input signal (see Fig.7)

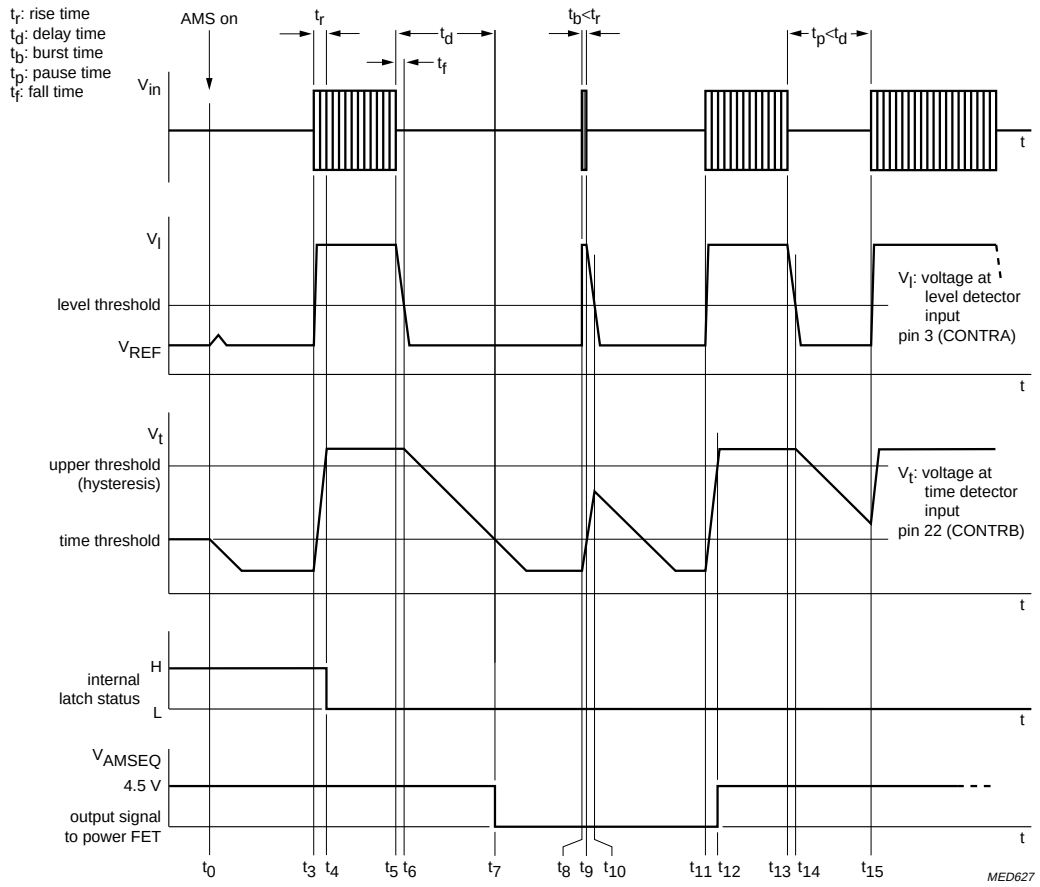


Fig.7 AMS-latch mode without initial input signal.

This is similar to the description of the principle timing diagram from AMS-scan mode. It only differs in its initial behaviour and its rise time t_r. (Please notice that the different t_r does not occur in the principle timing diagrams for latch and scan mode).

Running in AMS-latch mode, the circuit may be simply applied to drive a stop solenoid via a power FET. So the AMS output signal has not to be processed by a controller. Because there is no processor to make a decision whether there is a plop noise or not, for this mode the rise time t_r is extended to approximately 150 ms.

By activating AMS-latch mode the AMS output will not change to LOW level at t_2 if there is no initial signal at V_{in}.

A latch forces the AMS output to be HIGH until a signal appears at V_{in} (t_4). After t_4 the latch will not affect the output any more until AMS-latch mode is started again. The existence of the latch appears necessary if the AMS output for example drives a stop solenoid via a power FET. The LOW output level will cause a drive of the stop solenoid. This would happen after a maximum time of t_d occurred without any input signal. If there is no music on tape for a long time (e.g. at tape end), the AMS mode would be activated repeatedly as long as there is no signal at V_{in}. Thus the circuit waits until first music appears before detecting the pauses.

Description of the principle timing diagram for AMS-latch mode with initial input signal (see Fig.8)

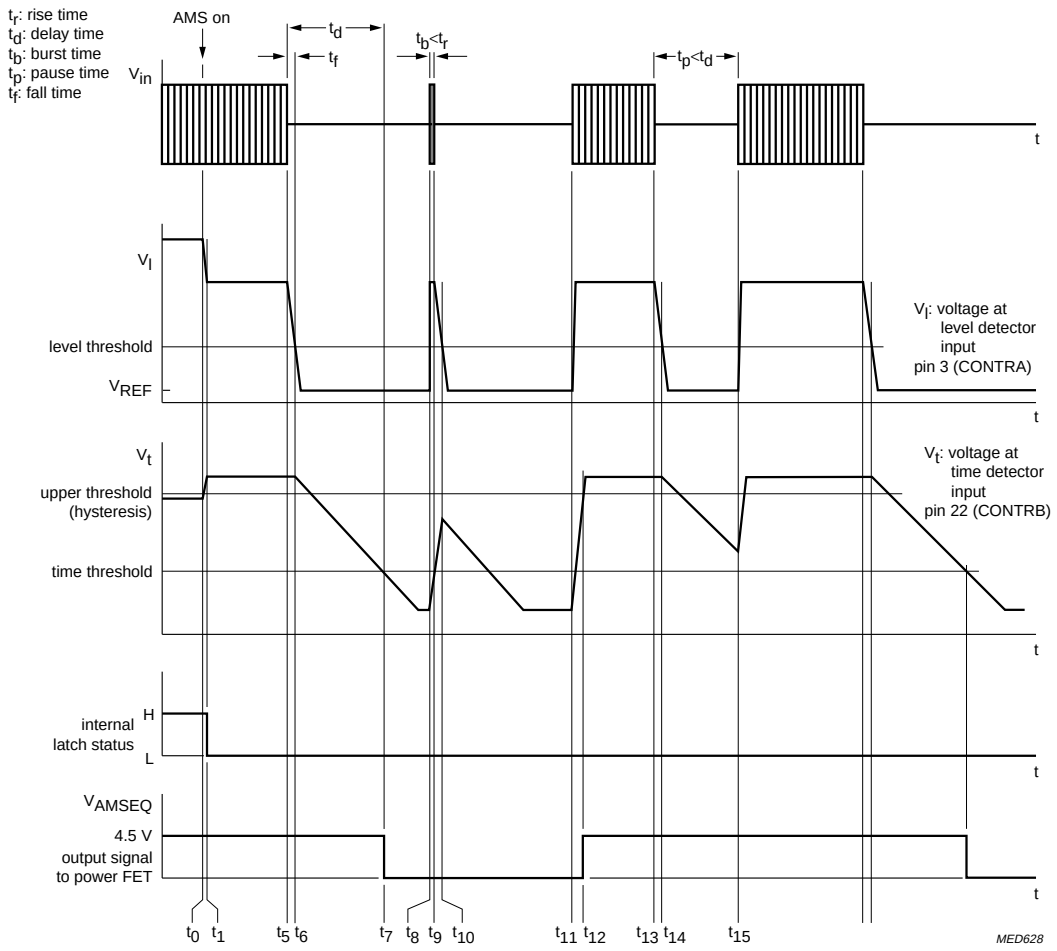


Fig.8 AMS-latch mode with initial input signal.

This is similar to the description in Section “Description of the principle timing diagram for AMS-scan mode with initial input signal (see Fig.6)”. It only differs in its rise time t_r and a release of its internal latch when voltage V_t passes the upper threshold between t_0 and t_1. Now the initial procedure is completed.

The following behaviour does not differ from the description in Section “Description of the principle timing diagram for AMS-latch mode without initial input signal (see Fig.7)”.

INTERNAL PIN CONFIGURATIONS

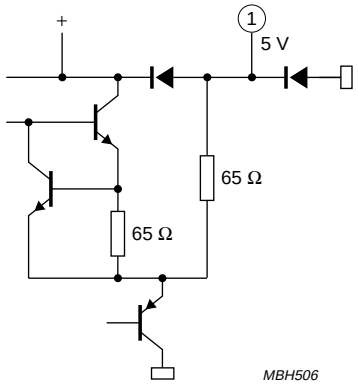


Fig.9 Pins 1 and 24: output channel.

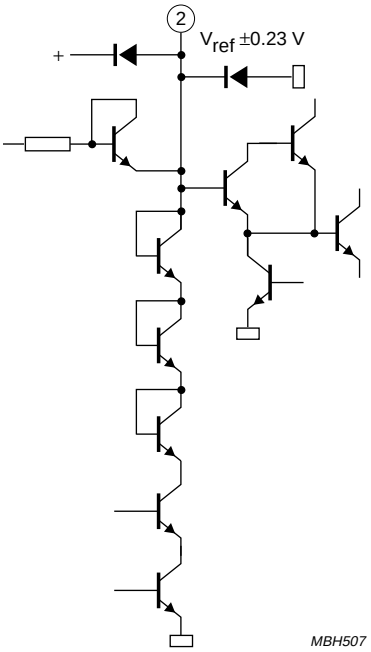


Fig.10 Pins 2 and 23: integrating filter.

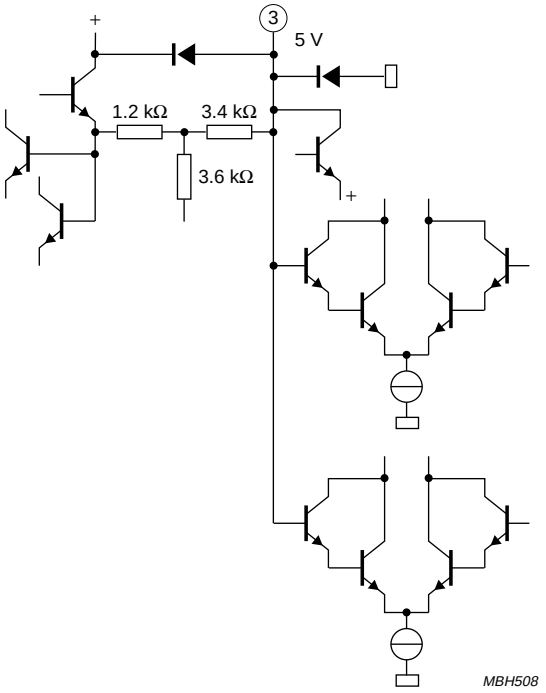


Fig.11 Pins 3 and 22: control voltage.

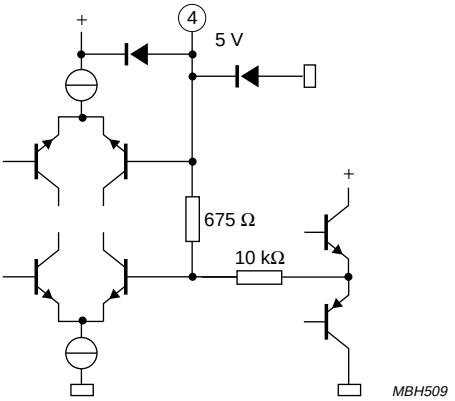


Fig.12 Pins 4 and 21: high-pass filter.

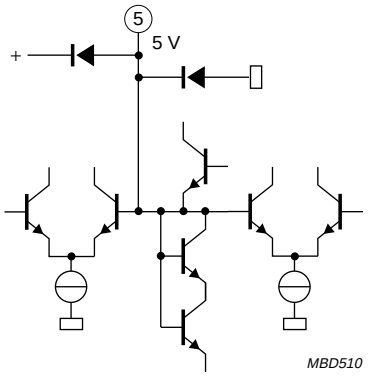


Fig.13 Pins 5 and 20: side chain.

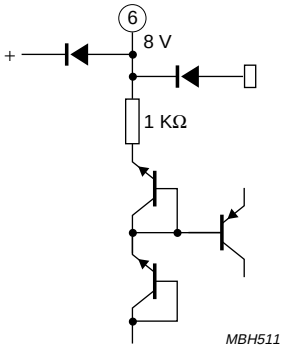


Fig.14 Pin 6: delay time constant.

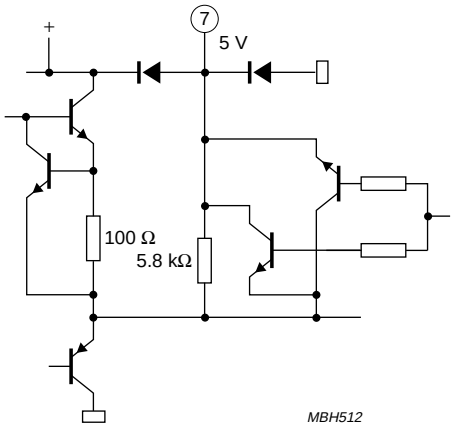


Fig.15 Pins 7 and 18: equalizing output.

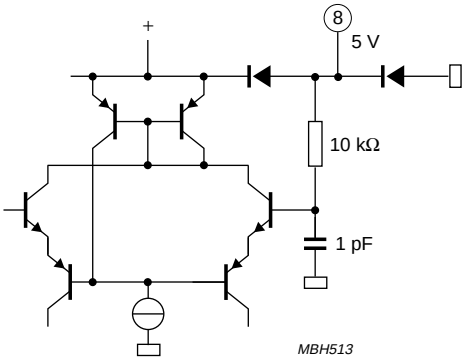


Fig.16 Pins 8 and 17: equalizing input.

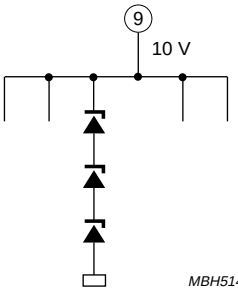


Fig.17 Pin 9: supply voltage.

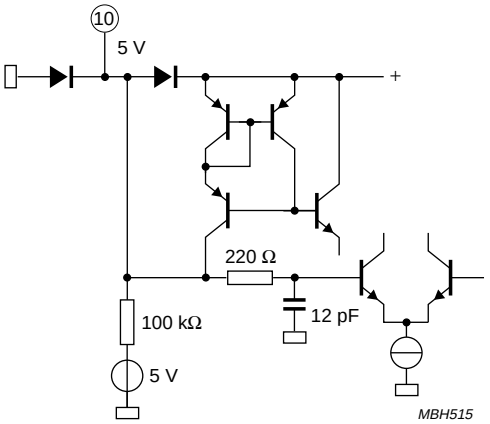


Fig.18 Pins 10, 12, 13 and 15: input channel.

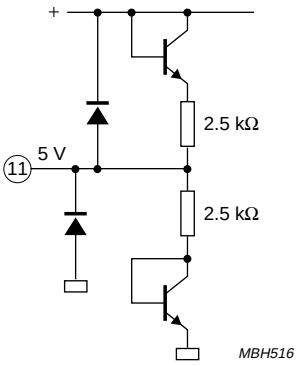


Fig.19 Pin 11: reference voltage.

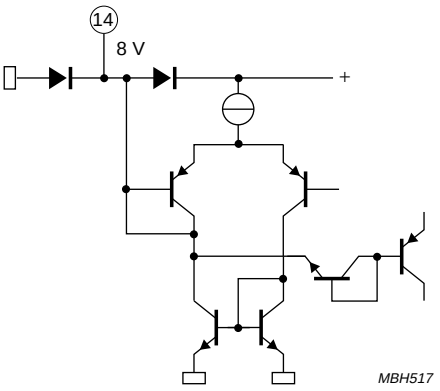


Fig.20 Pin 14: head switch input.

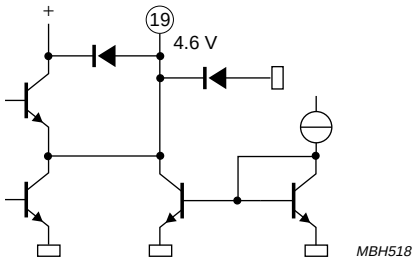


Fig.21 Pin 19: AMS output and EQ switch input.

TEST AND APPLICATION INFORMATION

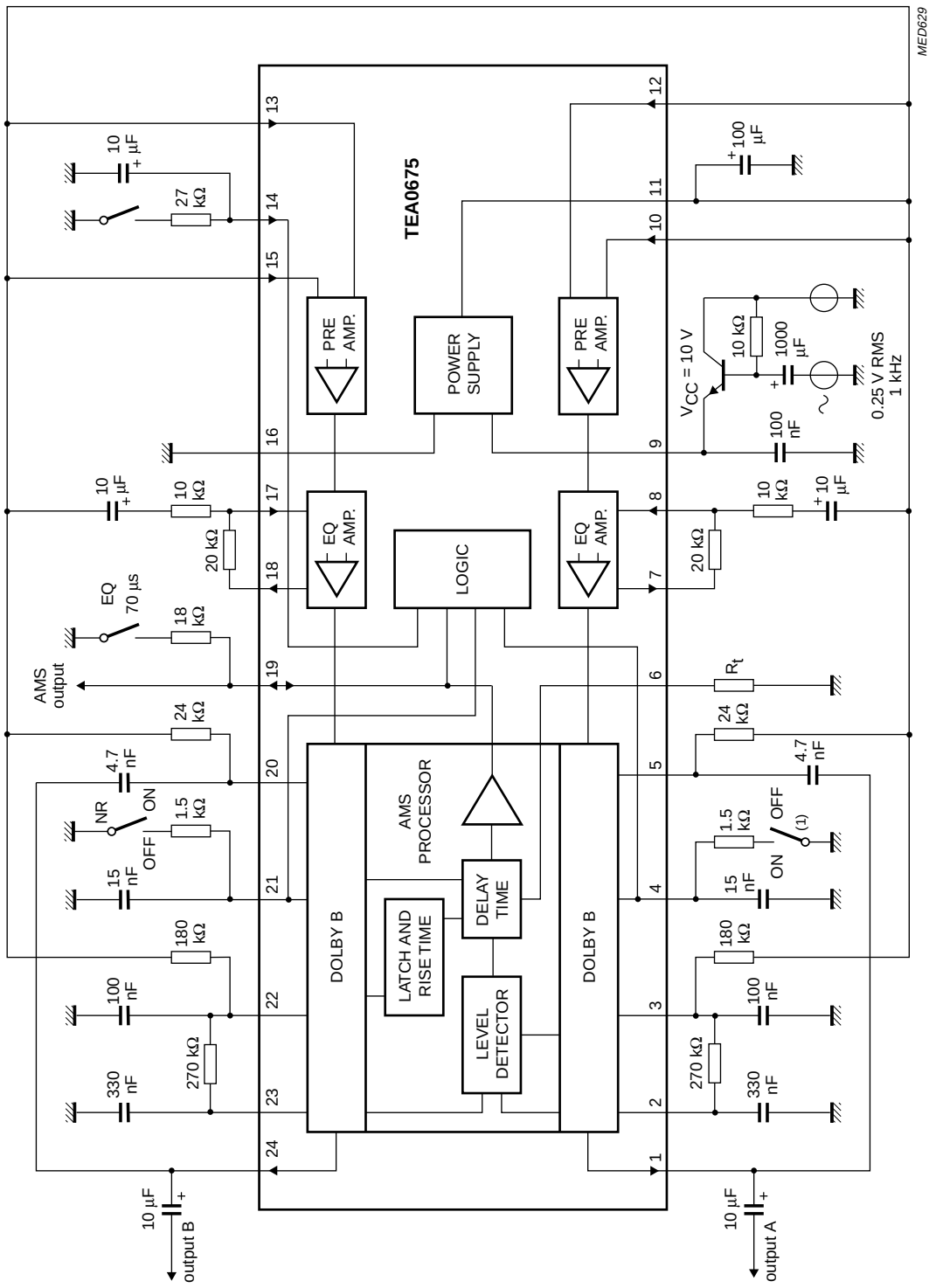


Fig.22 Test circuit for power supply ripple rejection.

(1) Switched to V_{CC} for AMS-scan mode.

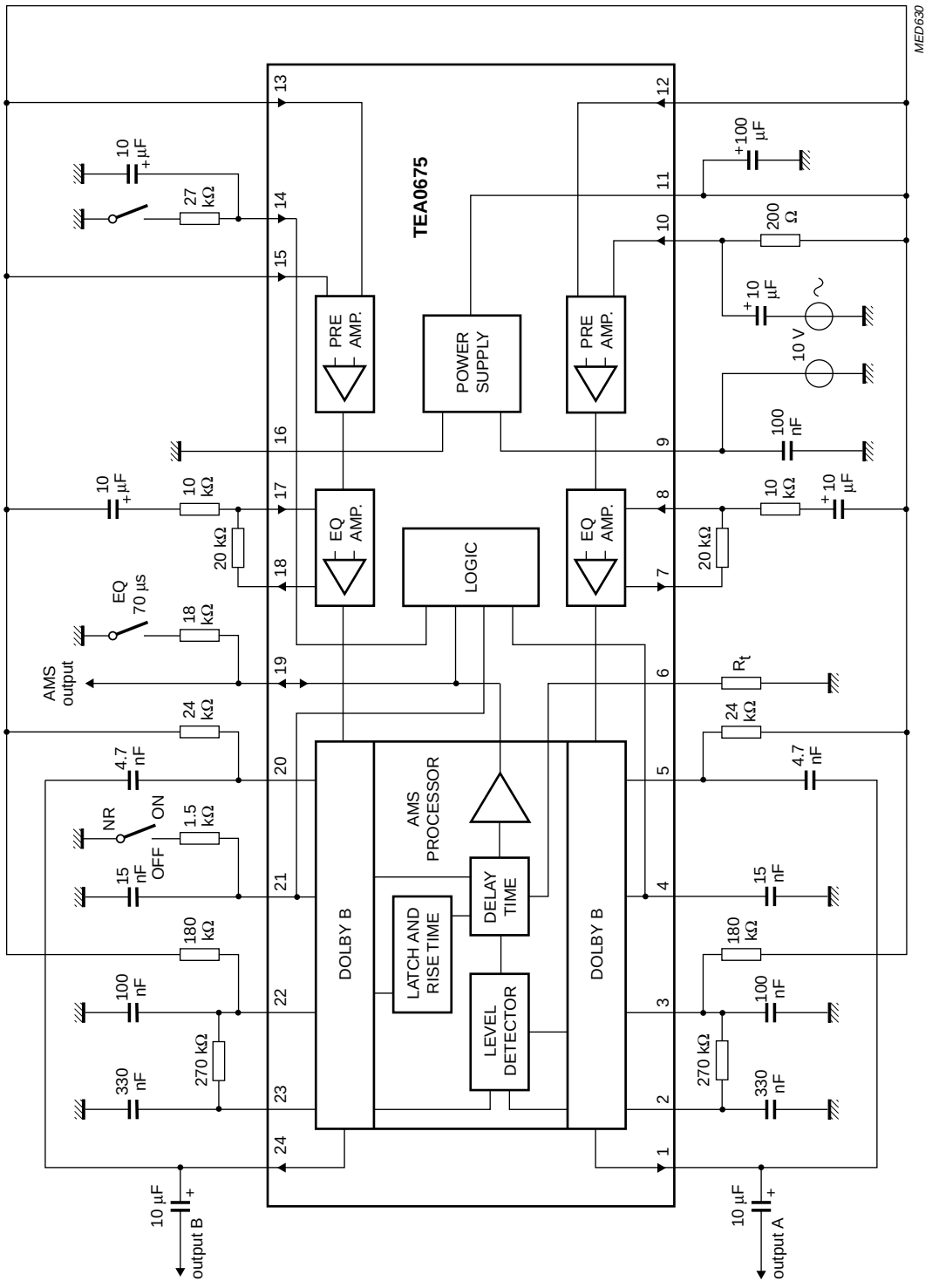


Fig.23 Test circuit for channel separation.

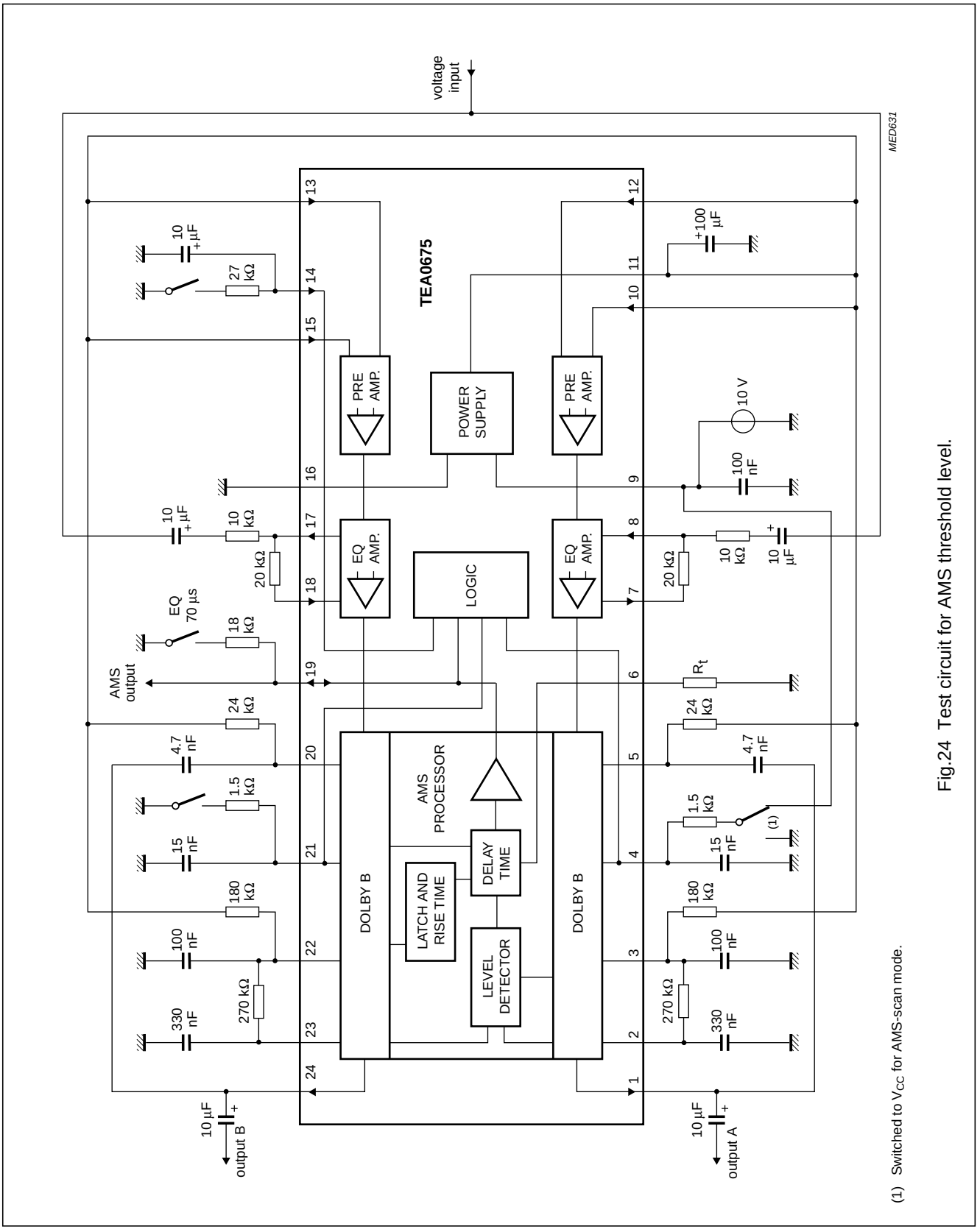


Fig.24 Test circuit for AMS threshold level.

(1) Switched to V_{CC} for AMS-scan mode.

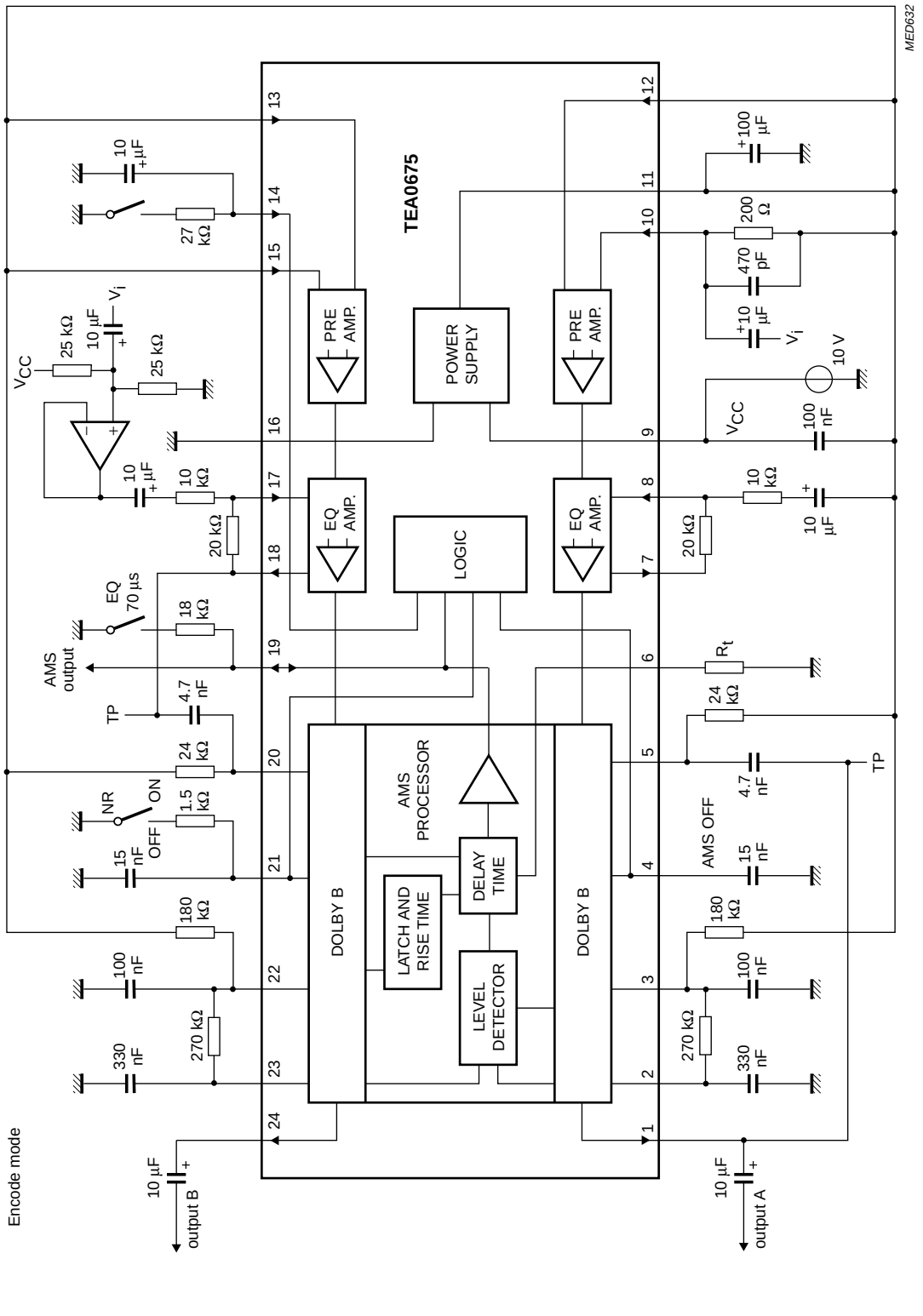


Fig.25 Test circuit for frequency response (channel B).

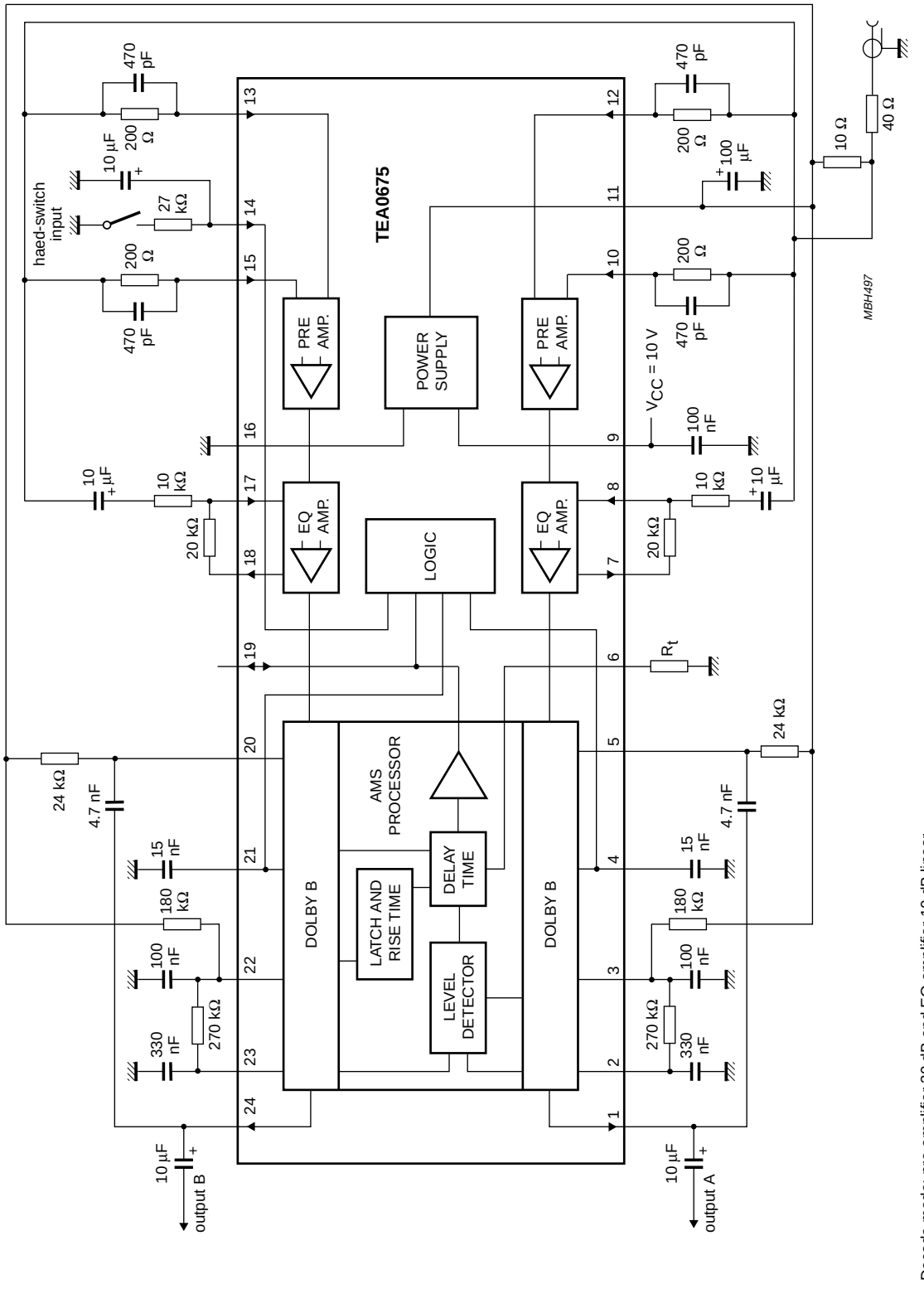
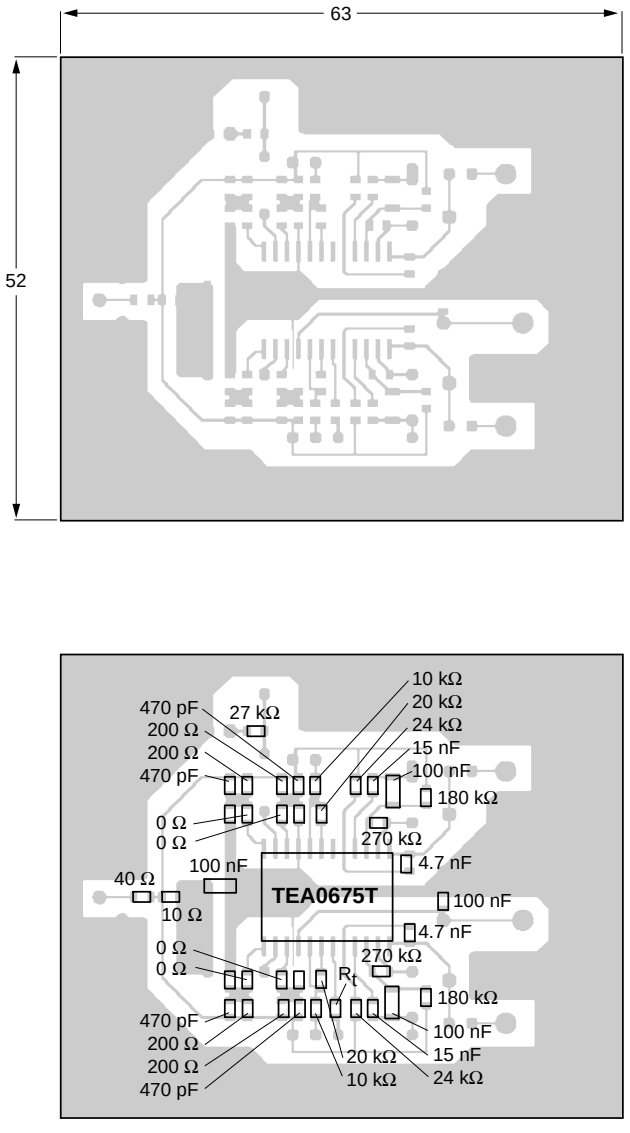


Fig.26 EMC test circuit.

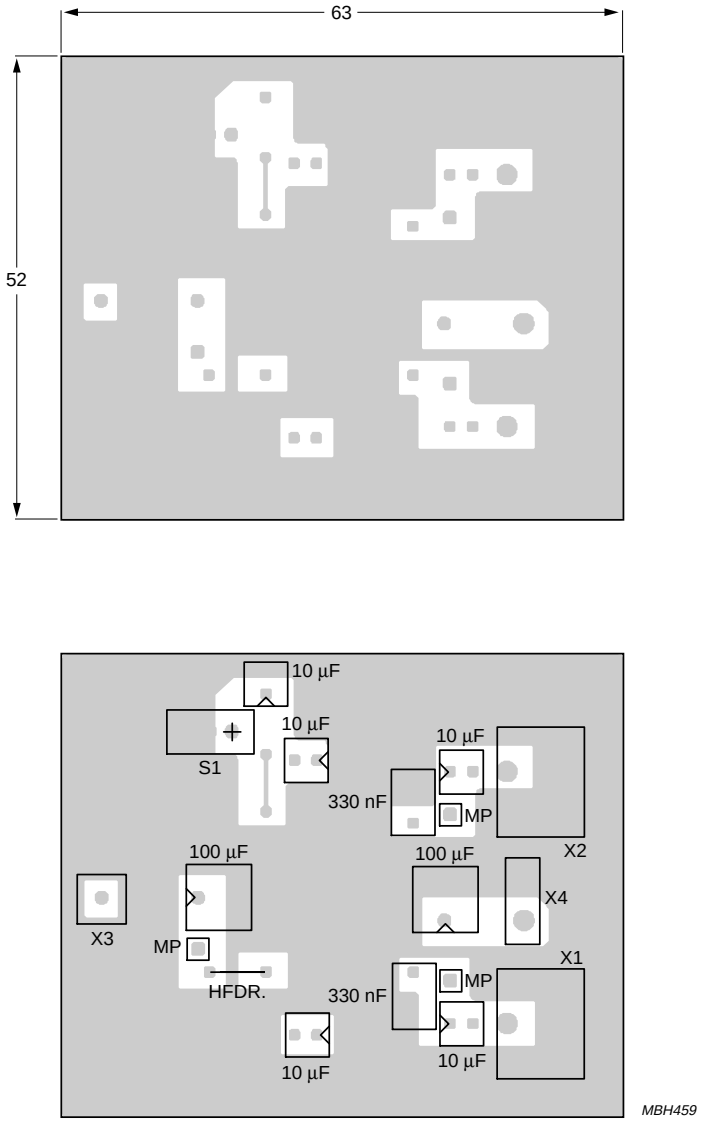
Decode mode: pre-amplifier 30 dB and EQ amplifier 10 dB linear.

LAYOUT OF PRINTED-CIRCUIT BOARD FOR EMC TEST CIRCUIT (FOR TEA0675T)



Dimensions in mm.

Fig.27 Top side with components.

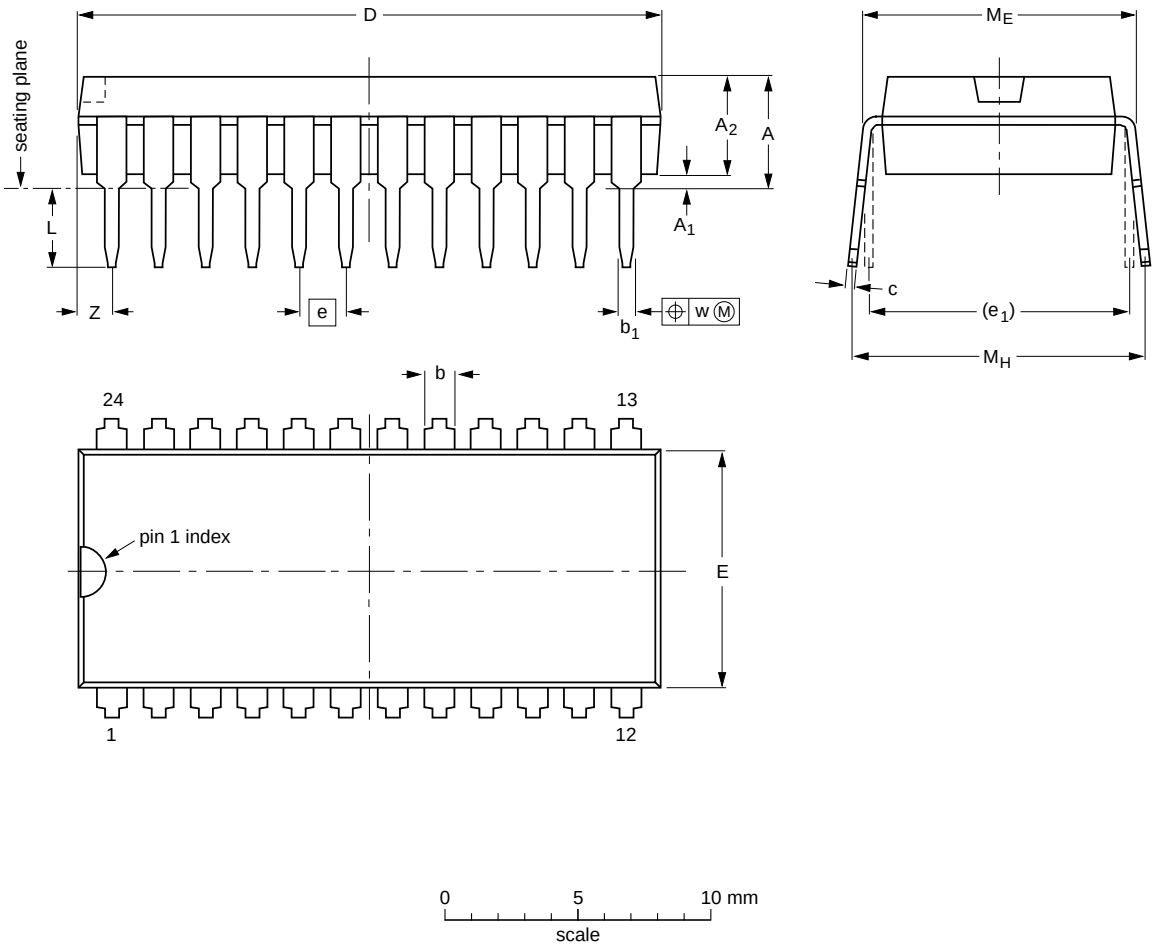


Dimensions in mm.

Fig.28 Bottom side with components.

PACKAGE OUTLINES

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

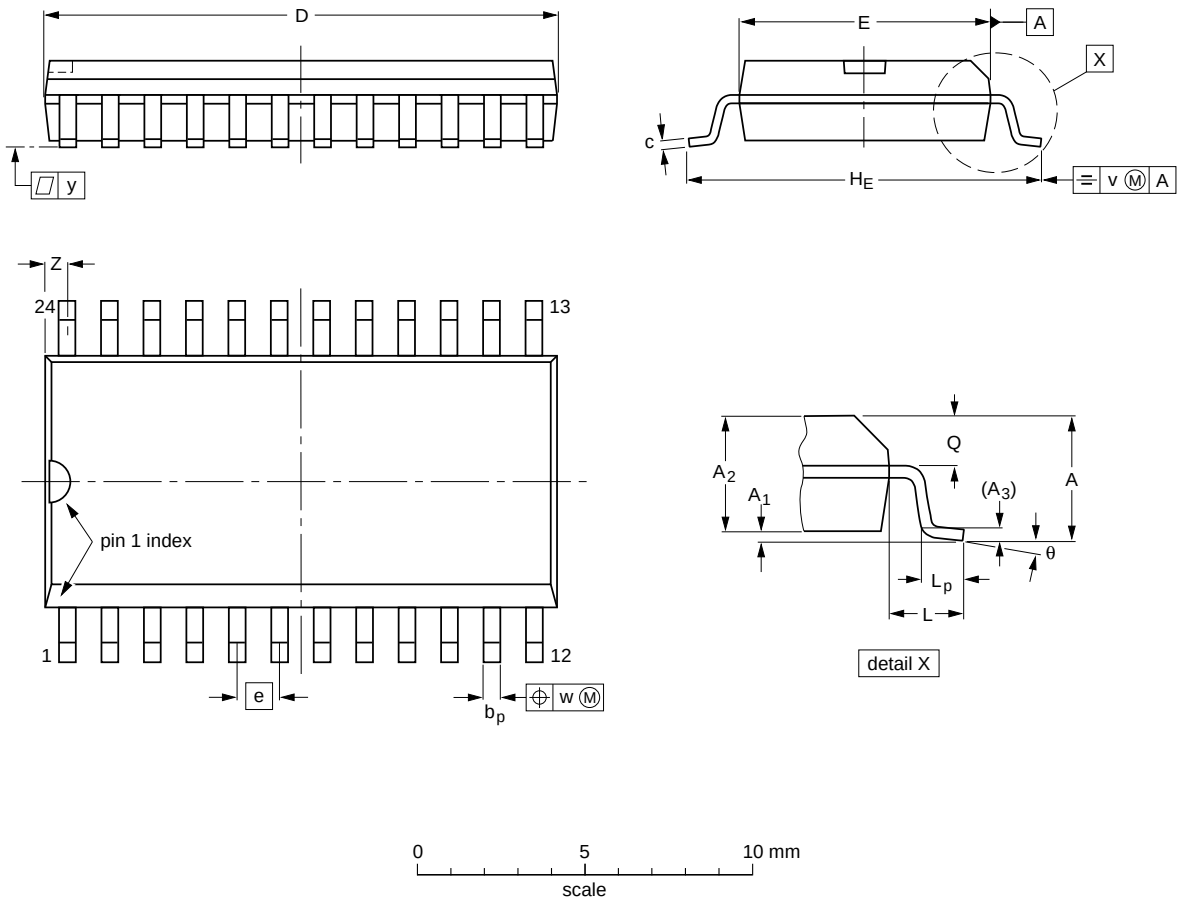
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

SDIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
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NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 805 4455, Fax. +61 2 805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 52 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 648 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 83749, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil, P.O. Box 7383 (01064-970),
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

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Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
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Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 2A Akademika Koroleva str., Office 165,
252148 KIEV, Tel. +380 44 476 0297/1642, Fax. +380 44 476 6991

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Uruguay: see South America

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